

Docket No.: 67161-086

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of : Customer Number: 20277  
:   
**Koichi ISHIMI** : Confirmation Number:  
:   
Serial No.: : Group Art Unit:  
:   
Filed: August 25, 2003 : Examiner:  
:   
For: INFORMATION PROCESSING APPARATUS WITH CLOCK GENERATING  
CIRCUIT AND INFORMATION PROCESSING APPARATUS WITH CLOCK  
DELAYING CIRCUIT

**INFORMATION DISCLOSURE STATEMENT**

Mail Stop IDS  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.


The relevance of the ten references listed on the attached Form 1449, is discussed in the present specification.

**Serial No.:**

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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SERIAL NO.

FILING DATE  
**August 25, 2003**

GROUP

## U.S. PATENT DOCUMENTS

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
		<b>Kouichi Ishimi et al., "A Full-Digital PLL for Low Voltage LSIs", Technical Report of IEICE, The Institute of Electronics, Information and Communication Engineers, ED97-45, SDM97-23, ICD97-35, June 1997, pp. 29-36</b>	
		<b>Michel Cmobes et al., " A Portable Clock Multiplier Generator Using Digital CMOS Standard Cells" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 31, NO. 7, July 1996, PP. 958-965</b>	

DATE CONSIDERED

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.